REMARKS

This paper is submitted in reply to the Office Action dated September 30, 2005, within the three-month period for response. Reconsideration and allowance of all pending claims are respectfully requested.

In the subject Office Action, the Examiner objected to the title as not being descriptive. Furthermore, claims 15 and 30 were rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Moreover, claims 1-31 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,594,712 to Pettey et al.

Applicants respectfully traverse the Examiner's rejections to the extent that they are maintained. Applicants have amended claims 1, 30 and 31. Applicants respectfully submit that no new matter is being added by the above amendments, as the amendments are fully supported in the specification, drawings and claims as originally filed.

Now turning to the subject Office Action, and specifically to the Examiner's rejection of the title, the Examiner will note that Applicants have amended the title as the Examiner requested to make it more descriptive.

Next turning to the §101 rejection, the Examiner apparently takes the position that the recitation of "program code" in claim 15 renders the claim non-statutory. Applicants respectfully traverse this rejection, however, in that even if "program code" was unstatutory by itself, claims are analyzed in their entirety when determining statutory subject matter, and in this regard, claim 15 recites an "apparatus," which is one of the statutory classes under 35 U.S.C. §101. Moreover, claim 15 recites a "processor," a hardware component that is unquestionably statutory in nature. When claim 15 is looked at in its entirety, the claim is statutory irrespective of whether "program code" by itself is statutory. Accordingly, withdrawal of the Examiner's §101 rejection of claim 15 is respectfully requested.

Next, with respect to claim 30, Applicants have amended this claim to recite a "tangible computer readable" medium. Moreover, claim 31 has been amended to clarify

that the computer readable medium includes "a recordable medium." In rejecting claim 30, the Examiner argues that a "program product" is non-statutory. Applicants respectfully traverse this rejection, as Applicants can cite literally thousands of issued United States Patents including claims of this nature. Nonetheless, as noted above, Applicants have amended claim 30 to clarify that the computer readable medium upon which the program code recited in claim 30 is bourne is a "tangible" medium, whereby claim 30 recites an article of manufacture-type claim including a tangible component. The incorporation of a tangible component into claim 30 renders the claim statutory, and as a result Applicants respectfully request withdrawal of the §101 rejection of claim 30.

Next turning to the art-based rejections, and specifically to the rejection of independent claim 1, this claim generally recites a method of allocating a memory address space to a plurality of Peripheral Component Interconnect (PCI) adapters coupled to a plurality of slots in a PCI bus. The method includes accessing configuration data associated with a slot identifier for each of the plurality of slots to determine a memory range size associated with each slot, and non-uniformly allocating memory address ranges to the plurality of PCI adapters based upon the memory range sizes associated with each slot.

The Examiner will note that claim 1 has further been amended to recite that non-uniform allocation of memory address ranges results in first and second adapters among the plurality of adapters that have the same connector type being allocated differently sized memory ranges. An important aspect of the invention recited in claim 1 therefore is the fact that different PCI adapters having the same connector type may be allocated differently-sized memory ranges based upon slot identifiers for the slots within which the PCI adapters are installed.

In rejecting claim 1, the Examiner relies on Pettey et al., and in particular, column 3, lines 52-54; column 7, lines 52-65; and column 9, lines 14-34. Of note, however, these passages in Pettey disclose, at the most, uniform allocation of blocks to address ranges

associated with remote Infiniband nodes, for use with direct remote direct memory access (DRDMA) operations. There is no disclosure in the reference of non-uniform allocation of memory address ranges based upon location, as is required by claim 1.

Specifically, Pettey discloses, at columns 7-9 and Figs. 3-6, a mapping of 4,096 byte address ranges with packet memory blocks (PMB's) that are used to build packets when communicating data between an Infiniband network and a PCI network. The PMB's are used to avoid having to double buffer data as it is being transmitted between the networks.

It is important to note, for example, that the passage cited at column 7, lines 52-65, which the Examiner analogizes to accessing configuration data associated with a slot identifier to determine a memory range size associated with each slot, the only configuration data that is disclosed is that of a base address register (DBAR) 322, which specifies a base address for DRDMA operations. As this register merely provides a base address, the register cannot be read to disclose "accessing configuration data...to determine a memory range size," as required by claim 1. Moreover, the passage does not disclose any configuration data that is "associated with a slot identifier for each of [a] plurality of slots." The DBAR register 322 provides a base address for a DRDMA PCI address space, and there is no disclosure in the reference that this address space is associated with any particular slot identifier.

In addition, the cited passage at column 9, lines 14-34 clearly discloses 32 DRDMA address ranges that are fixed at 4096 bytes each, which corresponds to the size of a payload region of each PMB. Furthermore, while Pettey recognizes at column 9, lines 30-32 that different sizes may be used, the reference does not state or imply that different sizes may be used for different address ranges in the same design. Indeed, as disclosed at column 18, line 62 to column 19, line 3, the assignment of address ranges to PMB's is random in nature, which necessarily requires that the address ranges all be the same size.

It is also apparent from reading Pettey that the size of each address range is static in nature, and not associated with any particular configuration data. The only configuration data referenced in the cited passages is a base address, which does not specify any particular size. As such, Applicants respectfully submit that Pettey does not disclose "accessing configuration data associated with a slot identifier for each of the plurality of slots to determine a memory range size associated with each slot," as is also required by claim 1.

Moreover, given that each address range used in Pettey is fixed in nature, and not dependent upon any configuration data, Pettey cannot be read to disclose "non-uniformly allocating memory address ranges to the plurality of PCI adapters based upon the memory ranges sizes associated with each slot." As noted above, each memory address range disclosed in Pettey is exactly 4,096 bytes in size, and consequently, to the extent that the assignment of address ranges in Pettey corresponds to "allocating memory address ranges," this allocation is uniform in nature. Furthermore, the allocation of memory address ranges performed in Pettey is to specific PMB's, and not any particular PCI adapters. Consequently, Pettey also fails to disclose this element of claim 1.

In addition, as noted above, claim 1 has been amended to further specify that the non-uniform allocation of memory address ranges is performed such that first and second PCI adapters among the plurality of PCI adapters that have the same connector type are allocated differently sized memory ranges. Given that Pettey does not disclose non-uniform allocation of memory address ranges, Applicants respectfully submit that Pettey cannot be read to disclose different PCI adapters having differently sized memory ranges allocated thereto. The cited passages also fail to address the concept of adapters having the same connector type being assigned different memory range sizes.

Accordingly, Applicants respectfully submit that claim 1 is novel over Pettey et al., and that the rejection should be withdrawn.

Applicants also submit that claim is non-obvious over Pettey and the other prior art of record, as there is no appreciation for the desirability of providing non-uniform allocation of memory address ranges to PCI adapters based upon the slot within which each adapter is installed. The Examiner has provided no objective evidence of a motivation to modify Pettey to utilize non-uniform allocation of memory address ranges, much less doing so based upon configuration data associated with slot identifiers for a plurality of slots. Accordingly, Applicants respectfully submit that claim 1 is also non-obvious over the prior art of record. Reconsideration and allowance of claim 1 are therefore respectfully requested.

Next, with respect to independent claim 2, this claim recites a method of allocating memory addresses to a plurality of input/output (IO) resources coupled to a plurality of IO endpoints in a memory mapped IO fabric, which includes determining a location in the memory mapped IO fabric for each IO endpoint among the plurality of endpoints, and non-uniformly allocating memory address ranges to the plurality of IO endpoints based upon the determined locations of the IO endpoints in the memory mapped IO fabric.

Therefore, similar to claim 1, claim 2 recites a non-uniform allocation of memory address ranges based upon location – in this instance, the location of IO endpoints in a memory mapped IO fabric.

Claim 2 is rejected based upon Pettey, and in particular, the passages at column 6, lines 20-39; column 9, lines 44-65; column 18, line 53 through column 19, line 23; and Fig. 1. None of these passages, however, discloses location-based, non-uniform allocation of memory address ranges to IO endpoints in a memory mapped IO fabric.

The passage at column 9, lines 44-65, which the Examiner asserts corresponds to the claimed feature of determining a location in the memory mapped IO fabric for each IO endpoint, merely describes the format of an address range register, which is used to map a DRDMA address range for a PCI burst address with a PMB such that burst data

can be routed directly to an appropriate buffer in the PMB. There is no disclosure in this passage corresponding to determining a location of an IO endpoint in a memory mapped IO fabric. Of note, it should be clear from a reading of Applicants' specification that the concept of determining a location of an IO endpoint refers to a network or bus location within the context of the IO fabric, rather than an address in a memory address space. While the Examiner is entitled to give the claim its broadest reasonable interpretation, and while the specification cannot be used to read subject matter into a claim, one of ordinary skill in the art would readily appreciate that Applicants' usage of the term "location" does not refer to a memory location, but rather a location of an IO endpoint in an IO fabric. The passage cited by the Examiner is relevant, if at all, to determining a memory location, i.e., an address, but is completely silent with respect to the location of an IO endpoint in an IO fabric. Therefore, Pettey does not disclose "determining a location in the memory mapped IO fabric for each IO endpoint among the plurality of endpoints," as required by claim 2.

Pettey et al. similarly does not disclose "non-uniformly allocating memory address ranges to the plurality of IO endpoints based upon the determined locations of the IO endpoints in the memory mapped IO fabric," as also required by claim 2. The passage cited at columns 18 and 19 discloses the mapping of address ranges to PMB buffers; however, this disclosure is irrelevant to claim 2 in that the PMB buffers are not "IO endpoints" (they are internal buffers in a transaction switch), and furthermore, as discussed above in connection with claim 1, the payload regions of the PMB's and the address ranges are each fixed at the same size (4,096 bytes) to enable the mappings therebetween to be randomly assigned. As such, no "non-uniform" allocation of memory address ranges is performed, much less performed specifically based upon the determined locations of the IO endpoints.

Accordingly, Applicants respectfully submit that claim 2 is novel over Pettey, and the rejection should therefore be withdrawn.

Moreover, claim 2 is non-obvious over Pettey in that there is no appreciation in Pettey or elsewhere in the prior art of the desirability of providing location-based, non-uniform memory allocation in a memory mapped IO fabric. Furthermore, the Examiner has provided no objective evidence that one of ordinary skill in the art would be motivated to modify Pettey to incorporate a non-uniform allocation of memory address ranges based upon the determined locations of IO endpoints in a memory mapped IO fabric. Accordingly, Applicants respectfully submit that claim 2 is also non-obvious over the prior art of record. Reconsideration and allowance of claim 2, as well as of claims 3-14 which depend therefrom, are therefore respectfully requested.

Next, with regard to independent claims 15 and 30, each of these claims likewise recites the concepts of determining a location in a memory mapped IO fabric for each IO endpoint among a plurality of IO endpoints, and non-uniformly allocating memory address ranges to the plurality of IO endpoints based upon the determined locations of the IO endpoints in the memory mapped IO fabric. Claims 15 and 30 are therefore novel and non-obvious over Pettey et al. and the other prior art of record for the same reasons as presented above with respect to claim 2. Reconsideration and allowance of these claims, and of claims 16-29 and 31 which depend therefrom, are therefore respectfully requested.

As a final matter, while Applicants traverse the Examiner's rejections of the dependent claims based upon their dependency on their respective independent claims, Applicants also wish to point out that a number of these claims recite additional subject matter that is further distinguishable from Pettey et al. and the other prior art of record.

For example, with regard to claims 3 and 16, the Examiner asserts that Pettey discloses determining the location and non-uniformly allocating memory address ranges during initialization of a memory mapped IO fabric. However, Applicants can find no disclosure of this concept in the cited passage at column 7, lines 29-65. Likewise, with regard to claims 4 and 17, the Examiner cites the same passage, yet the passage is entirely

silent with regard to the claimed concept of performing the aforementioned steps during initialization of a computer.

With regard to claims 5 and 18, which are directed generally to a logically-partitioned computer, and the performance of the aforementioned steps by a partition manager in a logically-partitioned computer, the Examiner cites column 7, line 66 to column 8, line 7. This passage does not discuss any computer architecture that is even arguably analogous to a logically-partitioned computer. The Examiner's attention is directed to pages 9-11 of the Application, which generally describe a logically-partitioned computer. In general, a logically-partitioned computer runs multiple partitions that operate as virtual computers, and that run separate operating system instances. The passage cited by the Examiner is entirely silent with regard to this concept.

With regard to claims 6 and 19, the Examiner cites column 7, lines 51-65 for allegedly disclosing the concept of allocating differently sized memory address ranges to IO endpoints having the same connector type. As Applicants have discussed above, Pettey discloses the allocation of fixed size address ranges (4096 bytes), and does not disclose the allocation of different sizes of memory address ranges to different endpoints. Furthermore, the concept of connector types is not addressed at all in the cited passage. Applicants therefore respectfully submit that Pettey cannot be read to disclose the allocation of differently sized memory address ranges to different IO endpoints.

With regard to claims 13 and 27, the Examiner alleges that Pettey discloses the allocation of a remaining memory address range to a last IO slot among a plurality of IO slots, citing column 9, lines 14-65. Applicants can find no disclosure in this passage regarding any special treatment of a last slot among a plurality of IO slots in regard to allocating memory thereto. Applicants respectfully submit that the cited passage is irrelevant to subject matter of these claims.

In summary, Applicants respectfully submit that all pending claims are novel and non-obvious over the prior art of record. Reconsideration and allowance of all pending

claims are therefore respectfully requested. If the Examiner has any questions regarding the foregoing, or which might otherwise further this case onto allowance, the Examiner may contact the undersigned at (513) 241-2324. Moreover, if any other charges or credits are necessary to complete this communication, please apply them to Deposit Account 23-3000.

Respectfully submitted,

15 DEC 2005
Date

Scott A. Stinebruner
Reg. No. 38,323
WOOD, HERRON & EVANS, L.L.P.
2700 Carew Tower
441 Vine Street
Cincinnati, Ohio 45202
Telephone: (513) 241-2324
Facsimile: (513) 241-6234